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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,412	09/28/2001	Richard L. Ford	042390.P11848	4354

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EXAMINER	
VU, TUAN A	

ART UNIT	PAPER NUMBER
2193	

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,412	FORD, RICHARD L.	
	Examiner	Art Unit	
	Tuan A. Vu	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-13 and 15-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-13 and 15-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 1/14/2005.

Claims 1, 11, 21 and 28 have been amended, claims 4, 14 canceled; and claims 1-3, 5-13, 15-28 resubmitted for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 10-13, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Buzbee, USPN: 5,815,720 (hereinafter Buzbee).

As per claim 1, Buzbee discloses a method comprising

receiving an application program (e.g. table 1 – col. 6; Fig. 2);

compiling the program into a first version, executing the first compiled version by a first processor, the compiling including instrumenting (e.g. col. 2, lines 19-34; col. 3, lines 49-55; *dynamic translator* – col. 6, lines 64 to col. 7, line 4; *annotations 42, 44* - Fig. 5) the first compiled version with monitoring instruction to direct the capture of profile data (Table 3, col. 7; table 5, col. 8);

executing the first compiled version using the first processor (e.g. *executed* - col. 3, lines 49-55);

capturing profile information during said execution (e.g. *Profile information 36* - Fig. 36); and

compiling the program into a second compiled version for execution by a second processor (e.g. *target computer* – col. 1, lines 22-24 – Note: optimizing a object code and target computer reads on execution by a second processor); the compiling of the second version including optimization based in part on the captured profile data (e.g. step 37- Fig. 2).

As per claim 2, Buzbee discloses captured data in memory (e.g. *will be used for future compilations* - col. 6, lines 18-24; col. 3, lines 12-16)

As per claim 3, see Buzbee (e.g. col. 1, lines 22-24).

As per claim 10, Buzbee discloses a one compiler to compile both profiling code and optimized code (e.g. Fig. 2, 5).

As per claim 11, this claim represents a computer-medium version of claim 1, and includes computer instructions for performing the same step limitations as recited therein; hence, is rejected using the corresponding rejections as set forth therein, respectively.

As per claims 12-13 and 20, these claims correspond to claims 2-3 and 10, respectively hence are rejected using the rejection as set forth therein, respectively.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buzbee et al., USPN: 5,815,720, as applied to claim 1, 11; in view of Schreiber et al. USPN: 6,507,947 (hereinafter Schreiber).

As per claim 9, Buzbee indicates a second or more compilation needed for further iterative recompiling to alleviate code size (col. 6, lines 4-28) but does not disclose having a second compiler to compile the first version of program using the profiling results. It was a well known concept to use more than one executing devices when resources are available to enable compiling/executing of complex or parallel iteration/execution, and this is shown in Shreiber (*parallel compilers* - Summary; Fig. 1, Fig. 14); and Buzbee discloses the loop iteration needed information for optimization (col. 7, lines 47 to col. 8, line 42); and in conjunction with possibilities to generate parallel code from complex nested loop as suggested, if resources are available - as mentioned above - such that more compilers are available, it would have been obvious for one of ordinary skill in the art at the time the invention was made to provide a second compiler in the iterative process of recompiling as endeavored by Buzbee because having any additional compiler needed for loop compiling or for iterative recompilation, this non-dependency of one compiler on another compiler executing apart from one another, as in parallel compiling to generate code for nested loops as taught by Shreiber, would expedite better results to help Buzbee purpose in satisfying the developer's intent to reduce size.

As per claim 19, this claim corresponds to claim 9, hence are rejected using the rejection as set forth therein.

6. Claims 5-8, 15-18, and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buzbee et al., USPN: 5,815,720, in view of Pegatoquet et al., USPN: 6,598,221 (hereinafter Pegatoquet).

As per claims 5, 6, 7, and 8, Buzbee discloses capturing of data and recompiling for an optimized object code for a target computer but does not teach a second processor being hosted

by the first processor, the second or target processor being a embedded processor not capable of capturing profile data or for generating external communications. Buzbee discloses that the first processor is providing optimized code for the second processor. But delivering optimized code via use of dynamic profile capture and annotation similar to Buzbee is further disclosed in the compiling method by Pegatoquet with a host system compiler for minimizing the target object code destined for a embedded DSP (e.g. Fig. 1-2). In view of Pegatoquet's host computer optimizing tool and communicating capabilities to enable code delivery to the DSP, it would have been obvious for one of ordinary skill in the art at the time the invention was made to use the compiler by Buzbee as host to embedded systems like the target DSP taught by Pegatoquet so that because of the well-known limited resources or communicating capabilities of most embedded devices, the host and its compiling capabilities would communicate with thus hosted embedded device for delivery of a optimized target code as intended by Buzbee's method, particularly to alleviate programmers work in writing code for DSP because of the increasingly complex software requirement to implement DSP (see Pegatoquet: BACKGROUND, col. 5, line 17 to col. 16, line 17).

As per claims 15-18, these claims correspond to claims 5-8, respectively hence are rejected using the rejection as set forth therein, respectively.

As per claim 26, Buzbee discloses a method of optimizing the execution of a program by an embedded processor, comprising:

obtaining a program, compiling the program to generate a first set of compiled code (e.g. Fig. 2, 5), such code being instrumented with instructions to monitor the execution of the first set of compiled code (e.g. col. 2, lines 19-34; col. 3, lines 49-55);

executing the first set of compiled code on a host processor; capturing profile information during such execution according to instrumented instructions of first set of compiled code (e.g. col. 2, lines 19-34; col. 3, lines 49-55; *dynamic translator* – col. 6, lines 64 to col. 7, line 4; *annotations 42, 44* - Fig. 5) and saving the profile information in a memory (see claim 2);

compiling the program to generate a second set of compiled code, the second set of compiled code being optimized based in part on the captured profile information (e.g. Fig. 2, 5); and

executing the second set of compiled code using the target processor (col. 1, lines 22-24).

But Buzbee does not disclose that the host processor is being contained in a device that also contains the target embedded processor. But in view of the teaching by Pegatoquet (see Fig. 1), the environment host system encompassing a target DSP device and operable to communicate optimized assembly code to a DSP target processor would have been obvious because of the direct communication of code and control as addressed in claims 5-8 above.

As per claim 28, refer to claim 10 for corresponding rejection.

7. Claims 21-25, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buzbee et al., USPN: 5,815,720, and Pegatoquet et al., USPN: 6,598,221; further in view of Schreiber et al. USPN: 6,507,947.

As per claim 21, Buzbee discloses a system comprising:

one or more memories, a first compiler compiling an application program into a first compiled version (Fig. 1; and related text), the compiling including instrumenting (e.g. col. 2, lines 19-34; col. 3, lines 49-55; *dynamic translator* – col. 6, lines 64 to col. 7, line 4; *annotations*

42, 44 - Fig. 5) the first compiled version with monitoring instruction to direct the capture of profile data (Table 3, col. 7; table 5, col. 8);

a microprocessor executing the first compiled version, the microprocessor capturing profile data during execution of the first compiled version (Fig. 2) according to the monitoring instruction instrumentation for the first compiled version (; *dynamic translator* – col. 6, lines 64 to col. 7, line 4; *annotations 42, 44* - Fig. 5); and

a target processor (col. 1, lines 22-24) and

compiling with a compiler the application code into a second compiled version, such version being optimized based in part of the captured profile data (e.g. Fig. 2,5).

But Buzbee does not teach a second compiler for compiling the application code into a second compiled version, the second version being optimized based on the captured profiling data. But this limitation of having a additional compiler to compile the first version would also have been obvious in light of the rationale as set forth in claim 9 above using parallel compilers or additional compiler to implement iterative recompilation in Buzbee's optimization.

Nor does Buzbee teach about hosting the target processor with the first microprocessor; but this host computer limitation to support embedded processor code generation has been addressed in claims 5-8 above.

As per claim 22, these claims correspond to claim 2 hence are rejected using the rejection as set forth therein.

As per claims 23-25, these claims correspond to claims 5-7, respectively hence are rejected using the rejection as set forth therein, respectively.

As per claim 27, the limitation as to use a second compiler has been addressed in claim 9 above; and is rejected herein using the corresponding rejection set forth therein.

Response to Arguments

8. Applicant's arguments submitted 1/14/2005 with respect to claim1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A. Vu whose telephone number is (272)272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571)272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAT
May 27, 2005

TODD INGBERG
PRIMARY EXAMINER